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8 IN THE UNITED STATES DISTRICT COURT
9 FOR THE NORTHERN DISTRICT OF CALIFORNIA
10

11 OKI AMERICA, INC. et al.,

No. C 04-03171 CRB

12 Plaintiff,

CLAIM CONSTRUCTION ORDER

13 v.

14 ADVANCED MICRO DEVICES, INC.,

15 Defendant.
16 _____/

17 This suit involves the alleged infringement of ten United States Patents. The patents
18 disclose devices and methods for use in the semiconductor industry. Now before the Court is
19 the task of interpreting the claims in six of these patents.

20 **DISCUSSION**

21 **I. DESCRIPTION OF THE PATENTS**

22 The six patents the parties have asked the Court to construe bear United States Patent
23 Numbers 5,739,571; 5,856,694 (collectively, the “Kurachi patents”); 5,338,986 (the
24 “Kurimoto patent”); 4,518,678 (the “Allen patent”); 4,960,732 (the “Dixit patent”); and
25 5,142,672 (the “Johnson patent”).

26 **A. Oki’s Patents**

27 The Kurachi and Kurimoto patents have been assigned to Plaintiff (“Oki”). ’694
28 Patent, at [73]; ’571 Patent, at [73]; ’986 Patent, at [73].

1 **1. The Kurachi Patents**

2 The Kurachi patents describe a integrated circuit in which one circuit, a “protection
3 MOSFET,” protects another circuit from electrostatic breakdown. ’571 Patent, at [57]. The
4 protection MOSFET turns on when static electricity contacts the integrated circuit. The
5 protection MOSFET absorbs the voltage created by the static electricity and shunts it towards
6 a ground, away from the other circuit. The parties ask the Court to construe the phrase
7 “protection MOSFETs.” Joint Claim Construction and Prehearing Statement, Ex. A (“Joint
8 Statement”) at 14.

9 **2. The Kurimoto Patent**

10 The Kurimoto patent also describes a circuit design that is resistant to damage caused
11 by voltage spikes. ’986 Patent, at [57]. The invention targets a specific problem known as
12 latch-up. Latch-up occurs when a circuit experiences a voltage spike that creates a low
13 resistance path through which a stray current flows directly from the power supply to the
14 ground. This stray current prevents the circuit from properly functioning and can
15 permanently damage the circuit. The Kurimoto patent prevents latch-up by introducing a
16 “resistive component” into a complementary metal oxide semiconductor (CMOS) transistor
17 circuit. *Id.* The parties ask the Court to construe the phrase “resistive component.” Joint
18 Statement at 12.

19 **B. AMD’s Patents**

20 The Allen, Dixit, and Johnson patents have been assigned to Defendant (“AMD”).
21 ’732 Patent, at [73]; ’672 Patent, at [73]; ’678 Patent, at [73].

22 **1. The Allen Patent**

23 The Allen patent describes a method for removing coating from the edges of a silicon
24 wafer. ’678 Patent, at [57]. The process removes the coating by placing a nozzle extremely
25 close to the edge of a spinning, circular wafer of silicon. The nozzle ejects solvent which
26 forms a “meniscus between” the spinning wafer and the nozzle. *Id.* at col.6 l.50. The parties
27 ask the Court to construe the phrase “whereby the meniscus provides a constant flow of said
28 chemical onto said substrate surface.” Joint Statement at 1.

2. The Dixit Patent

The Dixit patent describes a method of making a plug that creates an electrical connection between the metal wiring, or interconnect, in a semiconductor device and the transistor devices below. '732 Patent, at [57]. The plug stretches through a hole in an insulating layer sandwiched between the wiring and the devices. The metal wiring connects various transistors to each other to form integrated circuits. The plug connects the metal wiring to a region of the silicon wafer below that has been doped, or implanted with impurities, to increase its conductivity. Modern plugs are often made of Tungsten. However, chemical reactions that result from depositing the Tungsten can create two undesirable effects: wormholes, i.e. holes in the doped region of the wafer, and encroachment, i.e. holes between the insulating layer and the wafer. Furthermore, Tungsten does not adhere well to the wafer. To solve these problems, the patent suggests lining the socket with a thin "adhesion and contacting layer" and "barrier layer" before inserting the plug. *Id.* at col.7 ls.45, 50. The parties ask the Court to construe two phrases in the patent: (1) "forming an adhesion and contacting layer of titanium at least in said holes, including along said walls, in contact with the underlying doped region," and (2) "forming a contact plug comprising a conductive material which substantially fills said contact holes and which is in contact with said barrier layer." Joint Statement at 2, 5.

3. The Johnson Patent

The Johnson patent describes a method for allowing a computer's central processing unit ("CPU") to communicate with peripheral devices such as printers. '672 Patent, at [57]. Typically, the CPU and the peripherals are connected to each other by a bus. A bus is a collection of wires that can convey signals. The peripheral devices operate at slower speeds than the CPU. When the CPU is directly connected to these devices, the slower devices tend to limit the speed at which the CPU can operate. To remedy this problem, the patent describes a method for decoupling the CPU from the peripherals. First, the patent connects the CPU and other high-performing devices to a local bus. Then, the peripherals are connected to a remote bus. Two devices, an ("I/O") input/output port and a direct memory

access (“DMA”) channel, transfer data between the local bus and the remote bus. This arrangement allows data to flow from the CPU to the local bus, from the local bus to either the I/O port or to the DMA channel, from either of these devices to the remote bus, and from the remote bus to the peripherals. The patent requires “multiplexing” of the data before it is transferred from either the I/O port or the DMA channel to the remote bus. *Id.* at col.49 l.67. The parties ask the Court to construe the phrase “multiplexing address signals being transferred to said second bus by said access means and said controller means, together with data signals being transferred to said second bus.” Joint Statement at 7.

II. LEGAL STANDARD FOR CLAIM CONSTRUCTION

Patent infringement analysis involves two steps. The first step is to construe the asserted claims, and the second step is to determine whether the accused method or product infringes any of the claims as properly construed. *See Markman v. Westview Instruments, Inc.*, 52 F.3d 967, 976 (Fed. Cir. 1995) (en banc), *aff’d* 517 U.S. 370 (1996). The first step, construction of the patent claims, is a matter of law and thus the responsibility of the court. *See id.* at 979.

When construing the claims, a court first looks to the intrinsic evidence of record. *Vitronics Corp. v. Conceptor, Inc.*, 90 F.3d 1576, 1582 (Fed. Cir. 1996). The patent claims, specification, and the prosecution history constitute intrinsic evidence. *Id.* In most cases, the intrinsic evidence alone will determine the proper meaning of the claim terms. *Id.* at 1583. However, courts have discretion to admit and use extrinsic evidence. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1319 (Fed. Cir. 2005). “Extrinsic evidence consists of all evidence external to the patent and prosecution history, including expert and inventor testimony, dictionaries, and learned treatises.” *Markman*, 52 F.3d at 980. Extrinsic evidence is generally less reliable than intrinsic evidence. *Phillips*, 415 F.3d at 1318. Extrinsic evidence may not be used to contradict the meaning of the claim terms as defined by the claims themselves, specification, and prosecution history. *See id.* at 1319; *Vitronics Corp.*, 90 F.3d at 1584-85.

1 The language of the claims defines the scope of the invention. Vitronics Corp., 90
 2 F.3d at 1582. Generally, a court gives the words of a claim their ordinary and customary
 3 meaning. Phillips, 415 F.3d at 1312. The “ordinary and customary meaning of a claim term
 4 is the meaning that the term would have to a person of ordinary skill in the art in question at
 5 the time of the invention, i.e., as of the effective filing date of the patent application.” Id. at
 6 1313. The context in which a word appears in a claim informs the construction of that word.
 7 Id. at 1314. Other claims of a patent are valuable sources of information about the meaning
 8 of the term in dispute. Id. Normally, claim terms are used consistently throughout the patent.
 9 Id. “[T]he presence of a dependent claim that adds a particular limitation gives rise to the
 10 presumption that the limitation in question is not present in the independent claim.” Id. at
 11 1315.

12 In some cases judges need to look little further than the widely accepted meaning of a
 13 term. Where “the ordinary meaning of claim language as understood by a person of skill in
 14 the art [is] readily apparent even to lay judges” then “claim construction . . . involves little
 15 more than the application of the widely accepted meaning of commonly understood words.”
 16 Id. at 1313. In such cases, dictionaries may be especially helpful. Id. at 1314.

17 Claims must be read in light of the specification. Markman, 52 F.3d at 979. The
 18 specification “is the single best guide to the meaning of a disputed term.” Vitronics, 90 F.3d
 19 at 1582. “Usually, it is dispositive.” Id. If the patentee explicitly defined a claim in the
 20 specification, that definition trumps the ordinary meaning of the term. CCS Fitness v.
 21 Brunswick Corp., 288 F.3d 1359, 1366 (Fed. Cir. 2002). The specification may also define a
 22 term by implication. Phillips, 415 F.3d at 1321. The specification may reveal a disclaimer of
 23 claim scope by indicating that the invention and all of its embodiments only occupy part of
 24 the broad meaning of a claim term. SciMed Life Sys. v. Advanced Cardiovascular Sys., 242
 25 F.3d 1337, 1343-1344 (Fed. Cir. 2001).

26 However, it is error to import a limitation from the specification into the claim.
 27 Liebel-Flarsheim Co. v. Medrad, Inc., 358 F.3d 898, 904 (Fed. Cir. 2004). Standing alone,
 28 an embodiment disclosed in the specification does not limit the claims. Id. at 906.

Furthermore, the “fact that a patent asserts that an invention achieves several objectives does not require that each of the claims be construed as limited to structures that are capable of achieving all of the objectives.” Id. at 908. “To avoid importing limitations from the specification into the claims, it is important to keep in mind that the purposes of the specification are to teach and enable those of skill in the art to make and use the invention and to provide a best mode for doing so.” Phillips, 415 F.3d at 1323. Reading the specification in this context helps to clarify whether the patentee describes specific embodiments to accomplish those purposes or instead intends that the claims and the embodiments be strictly coextensive. Id.

A court “should also consider the patent’s prosecution history, if in evidence.” Markman, 52 F.3d at 980. “The prosecution history limits the interpretation of claim terms so as to exclude any interpretation that was disclaimed during prosecution.” Southwall Techs. v. Cardinal IG Co., 54 F.3d 1570, 1576 (Fed. Cir. 1995). However, because the prosecution history records a process of negotiation between the patentee and the PTO, it is often ambiguous. Phillips, 415 F.3d at 1317. Courts decline “to apply the doctrine of prosecution disclaimer where the alleged avowal of the claim scope is ambiguous.” Omega Eng’g, Inc. v. Raytek Corp., 334 F.3d 1314, 1324 (Fed. Cir. 2003). Where the prosecution history admits multiple interpretations of what the patentee intended the claim language to mean, the prosecution history does not limit the scope of the claims. Inverness Med. Switz. Gmbh v. Warner Lambert Co., 309 F.3d 1373, 1382 (Fed. Cir. 2002).

III. CONSTRUCTION OF DISPUTED TERMS IN THE PATENTS

The Court will begin its claim construction, as it must, with the intrinsic evidence: the patent claims, the specification, and the prosecution history. In every case, the intrinsic evidence determines the proper construction of the disputed terms.

A. The Kurachi Patents

The parties ask the Court to construe the phrase “protection MOSFETs” in Claim 1 of the ’571 Patent and Claim 1 of the ’694 Patent. Joint Statement at 14. The ’694 Patent is a continuation of ’571 Patent. For the Court’s purposes, the specifications of the two patents

are exactly the same. Furthermore, the first claims of each of the Kurachi patents share the same language. Thus, the Court's interpretation of the "protection MOSFETs" in the '571 Patent will govern the meaning of those terms in the '694 Patent.

The parties agree that MOSFET is an acronym for "metal oxide semiconductor field effect transistor." Oki's Opening Claim Construction Brief at 14; AMD's Markman Reply Brief at 4. The parties also agree that the "MOSFET" functions as a "protection MOSFET" because it is connected in a circuit in such a way that it protects against the excess surges resulting from electrostatic discharge. Oki's Opening Claim Construction Brief at 15; AMD's Markman Reply Brief at 3. The parties also agree that a protection MOSFET contains the following structural features: a source region, a drain region, a channel region, and a gate located above a thin insulating layer. Oki's Opening Claim Construction Brief at 17; AMD's Markman Reply Brief at 4.

The dispute centers around two issues. First, Oki protests defining the protection MOSFET in terms of its structural features. Oki's Opening Claim Construction Brief at 17. Second, AMD alleges that OKI disclaimed the use of PN diodes as protection MOSFETs during the prosecution of the Kurachi patents. AMD's Markman Reply Brief at 7. Oki does not deny that a disclaimer occurred, but it disputes the scope of that disclaimer. Oki's Claim Construction Reply Brief at 7. These disputes require the Court to answer two questions: (1) Should the Court omit from its definition the structures that both parties agree comprise a protection MOSFET? (2) Does the doctrine of prosecution history estoppel direct the Court to tack on to the end of its definition the sentence "[a] PN diode is not a MOSFET?" AMD's Markman Reply Brief at 4. The answers to those questions are no.

1. The Claims of the Kurachi Patents

The Kurachi patents describe a circuit device in which a "protection circuit" that contains "protection MOSFETs" protects another circuit, an "output buffer circuit," that contains "buffer MOSFETs" from "electrostatic breakdown." '571 Patent col.12 ls.34-37. The phrase "protection MOSFETs" appears twice in Claim 1. *Id.* at ls. 37 & 40. The first time it appears, the reader learns that the "protection circuit [has] protection MOSFETs,

1 including impurity diffusion layers, for preventing electrostatic breakdown of [the] buffer
 2 MOSFETs.” Id. at ls. 35-37. The second time it appears, the reader learns that the “buffer
 3 MOSFETs[, which have] impurity diffusion layers[, are] separated from [the] impurity
 4 diffusion layers of [the] protection MOSFETs by an interposed field oxide film.” Id. at ls.
 5 38-40.

6 The claims shed light on two features of the protection MOSFET. First, the claim
 7 language suggests what the word “protection” in the disputed phrase means. The MOSFETS
 8 are “protection MOSFETS” because they prevent electrostatic breakdown of the buffer
 9 MOSFETs. This notion is reinforced by the claim language describing the protection circuit
 10 that contains the protection MOSFETS. The invention has a “protection circuit for
 11 protecting said output buffer circuit.” Id. at ls.32-22. In both sentences, the protective
 12 function of the circuit and the MOSFET are immediately defined. These definitions also
 13 imply that the difference between a MOSFET and a protection MOSFET is not a structural
 14 difference, but a functional difference. This implication resonates with a definition of a
 15 protection MOSFET that includes the traditional structural features of a MOSFET.

16 The second limitation, that the “protection MOSFETS” include “impurity diffusion
 17 layers,” also suggests a definition that includes structure. A person of ordinary skill in the art
 18 in question at the time of the invention would know how a MOSFET typically functions. A
 19 MOSFET is formed within a silicon substrate. Oki’s Opening Claim Construction Brief, Ex.
 20 A (“Fair Decl.”) at ¶ 18. The source region, the channel region, and the drain region are
 21 embedded within the silicon substrate in that order. Id. Directly above the channel lies a thin
 22 layer of insulation. Id. The gate lies on top of the insulator. Id. When a threshold voltage is
 23 applied to the gate region, the gate metaphorically opens and current can flow from the
 24 source region to the drain region. See id. at 19. One skilled in the art would know that in
 25 order for the drain and gate regions to properly conduct electricity, they would have to be
 26 doped with impurities. See id. One skilled in the art would also know that an impurity
 27 diffusion layer refers to areas of the silicon substrate that have been doped with impurities.
 28 The patent claim language directs the Court towards two propositions. First, by referring to

the impurity diffusion layers, the claims themselves implicitly refer to the drain and gate regions of the protection MOSFET. Second, the claims indicate that a protection MOSFET may be defined by structure as well as function. Thus, the claims themselves refute Oki's argument that the MOSFET must be defined in a way that is devoid of structure.

2. The Specification of the Kurachi Patents

If there is any ambiguity left after reading the claims, the specification dispels it. The specification repeatedly refers to the structures that Oki wishes to banish from the definition. It indicates that the protection MOSFET has a "gate structure." '571 Patent col.3 l.46. On either side of the gate are electrodes that conduct current to the "source" and the "drain." Id. at l.52. Confirming what one skilled in the art already knew, the specification indicates that in various embodiments, the impurity diffusion layers act as the source and the drain of the protection MOSFETs. Id. at col.9 ls.23-25; col.6 ls.29-30; see id. at col.3 ls.50-53 (referring to drain and source electrodes that lie directly above the impurity diffusion layers). Confirming that these structures are not unique to the specific embodiments of the protection MOSFETs set forth, the specification also describes the buffer MOSFETs as having a "source," "drain," and "gate." Id. at col.3 ls.11-13, 18-21. Regardless of the type of MOSFET being described, the specification uses the same structural features to describe them. The Court will do the same.

3. The Prosecution History of the Kurachi Patents

AMD points to the prosecution history of the Kurachi patents to argue that the doctrine of file wrapper estoppel directs the Court to tack on to the end of its definition the sentence "[a] PN diode is not a MOSFET." AMD's Markman Reply Brief at 4. Were Oki attempting to define a protection MOSFET as a PN diode, they would be estopped from doing so because they disclaimed such an interpretation during prosecution. Claims 4 and 6 of the original Kurachi patent application claimed a "protection circuit having protective PN diodes." Oki's Claim Construction Reply Brief, Ex. A ("Kurachi Application") at 2. The Examiner rejected claims 4 and 6 as obvious over the prior art. AMD's Markman Reply Brief, Ex. 5 ("Kurachi Rejection") at 5. The Examiner noted that using the PN diode as a

1 protection device would have been obvious. Id. at 5-6. In response, Oki cancelled claims 4
 2 and 6. AMD's Markman Reply Brief, Ex. 6 ("Response to Kurachi Rejection") at 6, 20.
 3 Thus, the doctrine of file wrapper estoppel would prevent Oki from attempting to construe
 4 the protection MOSFETs of Claim 1 of the Kurachi patents as PN diodes.

5 However, the Court rejects as superfluous AMD's request that the definition of
 6 protection MOSFET include the sentence "[a] PN diode is not a MOSFET." First, Oki has
 7 not asked the Court to construe the protection MOSFET as a PN diode. To the contrary, Oki
 8 has admitted that "a MOSFET has a more complicated structure than a simple p-n junction."
 9 Oki's Opening Claim Construction Brief at 19. Second, including the structural elements of
 10 a protection MOSFET makes absolutely clear that a protection MOSFET involves more than
 11 a simple PN diode. Thus, the Court declines to define a protection MOSFET in terms of
 12 what it is not.

13 **4. Construction of Disputed Terms in the Kurachi Patents**

14 Based on the intrinsic evidence, the Court concludes that in the Kurachi patents a
 15 MOSFET, a metal oxide semiconductor field effect transistor, has a source region, drain
 16 region, channel region, and a gate located above a thin insulating layer. The Kurachi patents
 17 define a protection MOSFET as a MOSFET connected to a circuit in such a way that it tends
 18 to prevent one or more circuits from undergoing electrostatic breakdown.

19 **B. The Kurimoto Patent**

20 The parties ask the Court to construe the phrase "resistive component" in Claim 1 and
 21 6 of the Kurimoto Patent. Joint Statement at 10. AMD asks the Court to construe "resistive
 22 component" as a type of resistance. Id. Oki asks the Court to construe the term according to
 23 an abstract definition that is divorced from the language of the patent. See Oki's Opening
 24 Claim Construction Brief at 6. The Court chooses to define the disputed phrase as a type of
 25 resistance in accordance with the Kurimoto patent's idiosyncratic usage.

26 **1. The Claims of the Kurimoto Patent**

27 Taken out of context, Oki's definition of a resistive component as a component
 28 possessing the property of resistance to electrical current seems reasonable. However, a

1 close reading of the language and specification reveals that the patent defines the phrase by
2 implication.

3 The claims reveal the first cracks in Oki's definition. As noted above, the Kurimoto
4 patent prevents latch-up by introducing a "resistive component" into a complementary metal
5 oxide semiconductor (CMOS) transistor circuit. '986 Patent, at [57]. First, Claim 1 requires
6 that the "resistive component" be "provided" at the source of a "MOS transistor." Id. at col.5
7 ls.17-18. A MOS transistor is nothing more complicated than the MOSFET described in the
8 construction of the Kurachi patents. See Fair Decl. at ¶ 18. This limitation is consistent with
9 both Oki's and AMD's interpretation since either a component or a resistance could be
10 provided at the source of an MOS transistor.

11 Second, the "resistive component" must be "serially connected to a parasitic bipolar
12 transistor." '986 Patent col.5 ls.17-20. At first glance, this limitation seems to favor Oki's
13 definition because the phrase serially connected seems to indicate structures that are linked
14 together in a chain. However, Claim 11, using the same language as Claim 1, states that a
15 "parasitic resistance" must be "serially connected to a parasitic bipolar transistor." Id. at
16 col.8 ls.9-11. The parties agree that "parasitic resistance" as used in the Kurimoto patents is
17 defined as "a resistance in an integrated circuit that arises inherently due to the nature of the
18 materials used to implement the other elements of the integrated circuit." AMD's Markman
19 Reply Brief at 10; Oki's Claim Construction Reply Brief at 1. Thus, the claims indicate that
20 both a resistive component and a type of resistance may serially connect to a transistor. This
21 parallel language suggests that the patentee is using the disputed phrase to mean something
22 different from the meaning found in a regular dictionary.

23 The final claim limitation suggests that the resistive component has no separate
24 physical structure. Claims 1 and 6 require the "resistive component" to be "formed from a
25 layout in which a distance between a contact for [the] source of [a] MOS transistor[] and a
26 gate of [the] MOS transistor[] is longer than a distance between a contact for [the] drain of
27 [the] MOS transistor[] and the gate of [the] MOS transistor[]." Id. at col.5 ls.21-29; col.6
28 ls.29-36. The claim language indicates that the resistive component is not present as a result

1 of the addition of some external wire or body. Instead, the resistive component arises from
 2 rearrangement of the preexisting structures of the MOSFET. According to Claim 6, this
 3 same “asymmetry provid[es] a parasitic resistance.” Id. at col.8 ls.7-8. The claim language
 4 again uses that the phrases “resistive component” and “parasitic resistance” to mean the same
 5 thing.

6 2. The Specification of the Kurimoto Patent

7 The specification indicates the patentee uses the phrases resistive component and
 8 parasitic resistance interchangeably. Figure 3 of the patent illustrates a preferred
 9 embodiment of the invention. Id. at col.2 ls.13-15; 18-19. Referring to this figure, the
 10 specification describes exactly what gives rise to the “resistive component.”

11 As shown in FIG. 3, the arrangement of the contacts . . . is asymmetric with
 12 respect to the gate That is, in this layout of the CMOS output circuit, a
 13 distance between each [source] contact . . . and the gate . . . is longer than a
 14 distance between each [drain] contact . . . and the gate . . . , so as to render the
 15 resistive component . . . high.

16 Id. at col.4 ls.13-15; 18-19. If resistive component as used in the specification referred to a
 17 structure, the phrase “to render the resistive component” high would be nonsense. Nothing
 18 in the figure or the patent suggests that the resistive components are physically higher than
 19 other components in the patent. However, when resistive component is construed as a type
 20 of resistance, the sentence makes sense. According to this reading, placing the source
 21 contacts farther from the gate than the drain contacts raises the resistance.

22 Later, the specification again uses the phrase resistive component to refer to a type of
 23 resistance. Referring to an embodiment of Claim 5, the specification states that “the number
 24 of the contacts . . . on a side of the source . . . being less than the number of the contacts . . .
 25 on a side of the drain . . . increases the resistive component at the source.” Id. at col.4 ls.30-
 26 34. Again, this sentence only makes sense if “resistive component” is read to be a type of
 27 resistance. Read properly, the sentence indicates that having less source contacts than drain
 28 contacts increases the resistance at the source.

3. Construction of Disputed Terms in the Kurimoto Patent

The specification is dispositive. The Court holds that “resistive component” as used in Claims 1 and 6 of the Kurimoto patent refers to a resistance in an integrated circuit that arises due to the nature or layout of the materials used to implement the other elements of the integrated circuit.

C. The Allen Patent

The parties ask the Court to construe the phrase “whereby the meniscus provides a constant flow of said chemical onto said substrate surface” in Claim 5 of the Allen Patent. Joint Statement at 1. The parties agree that meniscus refers to the “curved surface of the solvent.” Oki’s Response to AMD’s Opening Markman Brief at 1; AMD’s Markman Reply Brief at 9. The parties also agree that a meniscus forms as a result of surface tension. AMD’s Markman Reply Brief at 9; see Oki’s Response to AMD’s Opening Markman Brief at 4.

Beyond that, the parties are at odds. Oki argues that the meniscus must extend “continuously from the nozzle tip to the substrate.” Oki’s Response to AMD’s Opening Markman Brief at 1. AMD’s definition only require the meniscus to form at the substrate. AMD’s Markman Reply Brief at 9. Oki argues that prosecution history estoppel places limits on the definition. Oki’s Response to AMD’s Opening Markman Brief at 1-3. The dispute again boils down to two issues. (1) Does Oki’s proposed requirement that the that the meniscus extend from the nozzle tip to the substrate have any support in the intrinsic evidence? (2) Does AMD’s decision to amend the claims to overcome a rejection place any limits on the scope of the claims? The answers to those questions are no and yes, respectively.

1. The Claims of the Allen Patent

Nothing in the claims supports the requirement that the meniscus be continuous and unbroken. The Allen patent describes a method for removing coating from the edges of a silicon wafer. ’678 Patent, at [57]. Claim 5 describes a process that involves “contacting one surface adjacent to the periphery of a [rotating wafer of] substrate with a chemical

capable of dissolving the coating material.” Id. at col.6 ls.48-50. This is accomplished “by forming a meniscus between [the] surface[of the substrate] and a nozzle positioned adjacent to the periphery of [that] surface.” Id. at ls.50-52. The claim then introduces the limitation in dispute: “whereby the meniscus provides a constant flow of said chemical onto said substrate surface.” Id. at ls.52-54. Thus, the claims impose three limitations on the meniscus. First, the formation of the meniscus must lead to the contact between the edge of the spinning wafer and the solvent. Second, the meniscus must form between the spinning wafer and the nozzle. Finally, the meniscus must provide a constant flow of the solvent onto the spinning wafer.

None of these requirements support Oki’s contention that the meniscus must extend continuously and unbroken from the nozzle tip to the substrate. In fact, the claims hint that such a requirement is unlikely. Oki’s requirement that the meniscus extend continuously and unbroken springs from a dictionary definition. That definition defines meniscus as “[t]he curved upper surface of a nonturbulent liquid in a container that is concave if the liquid wets the container walls and convex if it does not.” Oki’s Response to AMD’s Opening Markman Brief at 3 (quoting the American Heritage Dictionary (4th ed. 2000)) (internal quotations omitted). Oki then derives the continuous and unbroken requirement from the word nonturbulent. Id. at 3. However, in the Allen Patent, the meniscus does not exist in a stationary container. Instead, it exists between a nozzle out of which the solvent flows and a rotating wafer of substrate that is covered with a coating material. ’678 Patent col.6 ls.44-45, 56, 64-66. Given that the substrate is rotating, one would not expect the meniscus in the patent to replicate the behavior of a “nonturbulent liquid in a container.” The Court rejects Oki’s attempt to force the invention to behave in accordance with a dictionary definition that describes the behavior of a liquid in a context contrary to the plain language of the claims.

The claims also do not impose Oki’s requirement that the meniscus extend from the nozzle to the substrate. Oki’s logic proceeds as follows: (i) the definition refers to a single convex or concave surface between two stationary walls of a container; (ii) in the Allen patent, the liquid exists between the nozzle and the substrate; (iii) therefore, the meniscus

here must be one concave or convex surface between the nozzle and the substrate. Again, this logic suffers from the same fallacy: the claims indicate that the solvent does not lie stationary in a container but flows from a nozzle to the substrate. Furthermore, the word “between” in the claims only requires that the meniscus exist between the nozzle and the substrate, not extend like a bridge from one to the other. The Court finds no support in the claims for Oki’s requirement that the meniscus extend continuously and unbroken from the nozzle to the substrate.

2. The Specification of the Allen Patent

The specification also casts doubt on Oki’s attempt to impose its dictionary-based limitation on the claims. The specification refers to the meniscus twice. Referring to an illustration of the preferred embodiment, the specification describes how the meniscus forms. First, a valve is opened and the solvent flows under pressure from a reservoir through a series of tubes into the nozzle. Id. at col.3 ls.46-50. “As the chemical exits [the] nozzle . . . at [the] nozzle tip . . . , a meniscus is formed by the exiting liquid between [the] nozzle tip . . . and the underside of [the] substrate Forming of this meniscus is expedited by closely spacing [the] nozzle tip . . . to [the] substrate” Id. at col.3 ls.50-54. The specification reveals two important features of the meniscus. First, it may be formed by a liquid that is flowing under pressure. Second, moving the nozzle tip closer to the substrate expedites formation of the meniscus. The first limitation runs counter to Oki’s argument that the meniscus behave like a stationary liquid in a glass vessel. The second limitation is one that the parties conceded at oral argument when they both agreed that in order for the meniscus to form, the nozzle tip must be very close to the wafer.

3. The Prosecution History of the Allen Patent

The prosecution history sheds light on what the patent claims mean when they require that “the meniscus provide[] a constant flow of [the] chemical onto [the] substrate surface.” Id. at col.6 ls.52-54. During prosecution, the Examiner rejected all the claims of the Allen Patent as obvious or anticipated in light of the Sato patent. Oki’s Response to AMD’s Opening Markman Brief, Ex. 2 (“Allen Rejection”) at 1, 3. The Sato Patent teaches a

process similar to that of the Allen Patent. The Sato Patent describes a device that ejects liquid from a nozzle towards the edge of a spinning substrate to remove coating at the edge of the substrate. U.S. Patent No. 4,113,492 col.3 ls.28-47. However, nowhere does the Sato Patent mention a meniscus. Thus, AMD responded to the rejection by adding a new claim which eventually issued as Claim 5 of the Allen Patent. Oki's Response to AMD's Opening Markman Brief, Ex. 3 ("Response to Allen Rejection") at 5, 7. AMD distinguished the Allen Patent from the Sato Patent by pointing to the meniscus language at issue here. AMD stated that "[w]hile the applicant . . . does use a nozzle as does Sato, applicant's removal process comprises positioning the nozzle sufficiently close to the spinning coated wafer to establish a meniscus formed between the nozzle and the spinning wafer." *Id.* at 9. According to AMD, formation of this meniscus allows the invention to "control . . . the amount of surface contacted by the solvent solely by control of the rotational speed of the coated substrate." *Id.* at 12. AMD claimed that the Sato Patent neither anticipated nor made obvious this feature. *See id.* at 11-12. This exchange during the prosecution of the Allen Patent explains what the disputed claim terms mean. Because the meniscus provides a constant flow of the solvent onto the spinning wafer, the invention can control how much of surface area of the wafer the solvent contacts solely by varying the speed of rotation of the wafer. Thus, the claim limitation requiring the meniscus to provide a constant flow of the solvent onto the substrate distinguishes Claim 5 of the Allen patent over the Sato reference.

4. Construction of Disputed Terms in the Allen Patent

The intrinsic evidence directs the Court to construe the phrase "whereby the meniscus provides a constant flow of said chemical onto said substrate surface" of Claim 5 of the Allen Patent as follows. The meniscus, i.e., the curved surface of the chemical created by the surface tension of the chemical when the chemical contacts a solid, supplies a constant flow of the chemical onto the substrate. The meniscus exists between the nozzle and the substrate. The meniscus cannot form unless the nozzle is positioned sufficiently close to the spinning coated wafer.

D. The Dixit Patent: “Adhesion and Contacting Layer”

The parties ask the Court to construe two phrases in the patent. The first phrase, “forming an adhesion and contacting layer of titanium at least in said holes, including along said walls, in contact with the underlying doped region,” comes from Claim 1 of the Dixit patent. Joint Statement at 2. Based upon one of the advantages listed in the patent specification, Oki argues that the “adhesion and contacting layer” must cover the “entire insulating wall and the entire bottom of the contact hole without gaps.” Oki’s Response to AMD’s Opening Markman Brief at 14. Oki would also have the Court impose the limitation that the layer be composed of pure elemental Titanium. Id. The Court must resolve two issues: (1) Should the Court construe an advantage the Dixit patent recites as a limitation on the scope of the claim? (2) Does the Dixit patent forbid chemical reactions between the Titanium and the contact hole after the Titanium has been deposited in the holes. The answers to both questions are no.

1. The Claims of the Dixit Patent as They Relate to the “Adhesion and Contacting Layer”

The claims provide no support for either of the limitations Oki wishes to inject into the definition. Claim 1 describes a step-by-step process for manufacturing “contacts in an integrated semiconductor circuit.” ’732 Patent col.7 l.35. First, doped regions are provided in a semiconductor substrate. Id. at ls.37-38. Second, an insulating layer is laid down over the substrate. Id. at ls.39-40. Third, holes are made in the insulating layer above the doped regions. Id. at ls.41-44. Claim 1 refers to these holes as “contact holes.” Id. at l.41. Fourth, “an adhesion and contacting layer of titanium [is formed] at least in said holes, including along said walls, in contact with the underlying doped region.” Id. at ls.45-47. The “adhesion and contacting layer [must be] formed to a thickness insufficient to fill [the] contact holes.” Id. at ls.45-47. Fifth, a “barrier layer” is laid down on top of the “adhesion and contacting layer.” Id. at ls.50-51. Like the “adhesion and contacting layer,” the “barrier layer” cannot be so thick that it fills the hole. Id. at ls.51-52. Finally, a plug is formed in the contact holes. Id. at ls.54-55.

Nothing in the claims requires the adhesion and contacting layer to cover the entire insulating wall and the entire bottom of the contact hole without gaps. In fact, the claim language suggests otherwise. The adhesion and contacting layer only needs to “contact . . . the underlying doped region.” *Id.* at ls.47. The layer can contact the doped regions without covering it entirely. While slightly more ambiguous, the claim language “along said walls” does not necessarily require that the adhesion and contacting layer cover every exposed surface of the walls.

The claims are silent on what happens to the “titanium layer” after it has been formed in the contact holes. Of course, the claims require that the layer initially be formed of Titanium. What may happen after that only becomes clear upon reading the specification.

2. The Specification of the Dixit Patent as It Relates to the “Adhesion and Contacting Layer”

The fact that the Dixit patent asserts that the invention achieves several objectives does not require that Claim 1 be construed as limited to a process that is capable of achieving all of those objectives. The specification lists at least three advantages of a specific embodiment of the invention. The first is that while the material that forms the plug is being deposited into the contact holes, the chemicals “responsible for encroachment and worm hole generation never come into contact with the underlying silicon due to the presence of” the adhesion and contacting layer and the barrier layer. *Id.* at col.5 ls.34-36. Another advantage of the invention is that the plug can be doped with an opposite polarity to the doped regions in the substrate and the barrier layer will prevent the plug and doped regions from interacting. *Id.* at col.5 ls.39-45. Another advantage is that the barrier layer, since it contacts the interconnect layer, can conduct current if either the plug or the interconnect fails. *Id.* at col.5 ls.47-52. Oki wishes to convert the first advantage into a claim limitation. According to Oki, the first claim limitation implies that the adhesion and contacting layer can never have any gaps that allow the chemicals responsible for encroachment and wormholes to contact the underlying silicon.

1 This argument is wrong for two reasons. First, the fact that the Dixit patent asserts
 2 preventing these harms as one of several objectives does not require that Claim 1 be
 3 construed as limited to a process that is always capable of preventing those harms. Second,
 4 even if the Court were to convert the advantage into a claim limitation contrary to Federal
 5 Circuit law, the advantage only requires that the combination of the barrier layer and the
 6 adhesion and contacting layer prevent the undesired chemical reactions, not that the adhesion
 7 and contacting layer do so alone.

8 The specification also contradicts Oki's suggestion that the layer of Titanium must
 9 never react with chemicals in the substrate to form other compounds. The specification
 10 refers to a combination of a Titanium (Ti) adhesion and contacting layer and a Titanium
 11 Nitride (TiN) barrier layer as "Ti/TiN." Id. at col.6 ls.31-33. The specification then
 12 describes the one way to lay down this "titanium/titanium nitride bilayer." Id. at ls.58-59.
 13 After describing the process, the specification notes "that in the Ti/TiN process, one
 14 substantially obtains $TiSi_{[sub]x}$ contact silicidation where titanium contacts the junction."
 15 Id. at ls.58-59. Thus, the specification clearly states that as the Titanium adhesion and
 16 contacting layer is formed, the chemical reaction silicidation occurs resulting in the product
 17 $TiSi_{[sub]x}$. The specification also states that if the Titanium adhesion and contacting layer is
 18 too thick, it "may consume unacceptable amounts of silicon from the junctions due to
 19 titanium silicide formation." Id. at col.4 ls.32-33. Contrary to Oki's argument, this suggests
 20 that silicidation always occurs and that its by product reaches unacceptable levels in certain
 21 circumstances.

22 3. Construction of Disputed Terms in the Dixit Patent

23 Here, the language of the claims and the specification is dispositive. The Court
 24 construes the phrase "forming an adhesion and contacting layer of titanium at least in said
 25 holes, including along said walls, in contact with the underlying doped region" of Claim 1 to
 26 require that Titanium be deposited in the contact holes so as to form an adhesion and
 27 contacting layer. This layer runs along the walls of the holes and contacts the underlying
 28 doped regions.

D. The Dixit Patent: “Contact Plug”

As noted above, the parties ask the Court to construe two phrases in the patent. The second phrase, “forming a contact plug comprising a conductive material which substantially fills said contact holes and which is in contact with said barrier layer,” also comes from Claim 1 of the Dixit patent. ’732 Patent col.7 ls.54-56. The parties agree that the plug substantially fills the contact holes. Oki’s Response to AMD’s Opening Markman Brief at 9; AMD’s Markman Reply Brief at 6. The parties further agree that the plug is made of a conductive material. Oki’s Response to AMD’s Opening Markman Brief at 9; AMD’s Markman Reply Brief at 6.

The Court must resolve one issue. The parties disagree over whether AMD disclaimed a plug that forms one, continuous structure with a metal interconnect that lies over the hole. Thus, the Court must decide whether an ambiguous reference to a prior art patent during the prosecution history disclaims subject matter that unambiguously falls within the scope of the claims and specification. It does not.

1. The Claims of the Dixit Patent as They Relate to the “Contact Plug”

The doctrine of claim differentiation indicates that Claim 1 contemplates a plug that forms a continuous unit with the interconnect that lies above it. The plain language of Claim 1 itself does not require the plug to be separate from the interconnect above. Claim 1 merely requires that the plug (1) substantially fill a contact hole and (2) contact the barrier layer that lies directly beneath it. ’732 Patent col.7 ls.55-56. Claim 11 of the Dixit patent ultimately depends from Claim 1. Id. at col.8 ls.14,18. In Claim 11, the “conductive material [that formed the plug of Claim 1] is etched back to expose [the] barrier layer on [the] insulating layer but leaving [the] conductive layer substantially filling [the] contact hole, thereby preserving [the] contact plug.” Id. at ls.19-22. Claim 11 then goes on to recite laying down the interconnect directly above the contact plug. Id. at ls.23-29. This claim language shows that within the scope of Claim 1 lies a plug that forms one continuous piece with the interconnect above. The process of Claim 11 then etches back the portion of the plug that sticks out above the top of the contact hole. Then, the interconnect is laid down on top of the

1 etched back plug. Thus, the presence of the limitation in dependent Claim 11 that the plug be
 2 formed separately from the metal interconnected over the hole implies that this limitation is
 3 not present in the Claim 1.

4 Claim 13, which also ultimately depends from Claim 1, expressly describes a plug that
 5 forms ones continuous unit with the interconnect above. Id. at ls.14, 33-24. Claim 13 recites
 6 a process in which the

7 conductive material [that forms the plug] and [the] underlying barrier layer and
 8 adhesion and contacting layer are patterned and etched to expose portions of
 9 [the] insulating layer, leaving defined patterns of [the] conductive material and
 10 [the] barrier layer and [the] adhesion and contacting layer forming interconnect
 11 regions, with [the] interconnect regions at least partially overlying [the] contact
 12 holes.

13 Id. at col.8 ls.33-41. Claim 13 envisions a process in which a continuous plug and
 14 interconnect (and the barrier and adhesion and contacting layers below it) are etched back to
 15 expose part of the insulating layer. However, the etching stops before the entire portion of
 16 the plug that juts out of the top of the contact hole is etched away. This leaves a plug that
 17 forms one continuous unit with the interconnect above. Because Claim 13 depends from
 18 Claim 1, it is presumed to fall within the scope of Claim 1. Thus, Claim 1 includes a plug
 19 that may be formed continuously with the metal interconnect over the hole.

20 **2. The Specification of the Dixit Patent as It Relates to the “Contact** 21 **Plug”**

22 The specification of the Dixit patent also describes plugs that extend outside of the
 23 contact holes to form part of the overlying interconnect. In fact, the very first figure in the
 24 patent depicts such a plug. Id. at fig.1A. Describing this picture, the specification indicates
 25 that “[s]ince the resistivity of tungsten is low enough that it could be used as an interconnect,
 26 one could pattern the as-deposited tungsten layer . . . to form the interconnect.”

27 Id. at col.5 ls.53-56. Other parts of the specification also envision a plug that forms one
 28 piece with the interconnect. Id. at fig.2; col.2 ls.57-59. Thus, the claims and the

specification unambiguously include within their scope a plug that forms one piece with the interconnect.

3. The Prosecution History of the Dixit Patent as It Relates to the “Contact Plug”

Oki attempts to squeeze a disclaimer of claim scope from the prosecution history. This attempt fails because the alleged avowal of the claim scope during prosecution is too ambiguous to amount to a disclaimer. During the prosecution of the Dixit patent, the Examiner described the Mori patent as “relevant prior art.” Oki’s Response to AMD’s Opening Markman Brief, Ex. 6 (“References Cited by Examiner”) at 4. The Examiner did not reject the Dixit patent over the Mori patent. Instead, the Examiner explained that the Mori reference was relevant because “it shows a first Ti layer then a barrier layer deposited before connecting with aluminum.” *Id.* The Examiner then went on to state that “there is no plug” in the Mori patent. *Id.* In response, Dixit stated that “[t]he Examiner correctly notes that there is no plug present.” Based on this exchange, Oki argues that the plug in the Dixit patent cannot form one piece with the metal interconnect above. Oki asks for too much. Nothing in the text of this exchange indicates that the Examiner or the patentee believed that it was distinguishing the Dixit patent over the Mori patent based on the lack of a unitary plug-interconnect structure in the Dixit patent.

Because the prosecution history admits multiple interpretations of what the patentee intended the claim language to mean, the prosecution history does not limit the scope of the claims. The prosecution history does not reveal why the patentee and the Examiner thought that Mori did not contain a plug. If fact, the prosecution history does not even indicate whether the patentee and the Examiner agreed on the reason the Mori patent did not contain a plug. Oki submits expert testimony claiming that the reason there was no plug is that the Mori reference depicts a one-piece metal interconnect and plug (for lack of a better word)¹. Oki’s Response to AMD’s Opening Markman Brief, Ex. 9 (“Fonash Decl.”) at ¶ 16. AMD

¹ In rebuttal, AMD submits expert testimony claiming that a plug can form one piece with the overlying interconnect. AMD’s Opening Markman Brief, Ex. 3 (“Neikirk Decl.”).

1 submits expert testimony that supports its argument that the contact holes in the Mori patent
 2 were too wide and shallow to have been considered plugged by one skilled in the art². See
 3 AMD's Markman Reply Brief at 7 (citing AMD's Opening Markman Brief, Ex. 4 ("Fonash
 4 Deposition")) at 87-88). Both interpretations of the prosecution history are plausible. Neither
 5 of them appear in the prosecution history itself. The Court will not knit a prosecution history
 6 disclaimer from the yarn provided by experts.

7 **4. Construction of Disputed Terms in the Dixit Patent**

8 Because the prosecution history does not reveal an unambiguous disclaimer of the
 9 scope of the claims, the Court construes the phrase "forming a contact plug comprising a
 10 conductive material which substantially fills said contact holes and which is in contact with
 11 said barrier layer" of Claim 1 of the Dixit patent as follows: The hole is plugged and thereby
 12 substantially filled with a conductive material. This plug is in contact with the barrier layer.

13 **E. The Johnson Patent**

14 The parties ask the Court to construe the phrase "multiplexing address signals being
 15 transferred to said second bus by said access means and said controller means, together with
 16 data signals being transferred to said second bus" in Claim 55 of the Johnson patent. Joint
 17 Statement at 7. The parties agree that in the abstract "multiplexing" by itself can refer to (1)
 18 selecting one of two sets of data from an input for transmission to an output and (2)
 19 interleaving the two sets of data in time for sequential transmission to an output³. AMD's
 20 Opening Markman Brief at 23; Oki's Response to AMD's Opening Markman Brief at 25.
 21 However, Oki argues that in the context of the Johnson patent, multiplexing requires
 22 interleaving two sets of data for transmission to an output. Oki's Response to AMD's
 23

24 ² In rebuttal, Oki points to expert testimony suggesting that AMD's expert could not tell
 25 how wide and shallow the contact hole in Mori was. Oki's Response to AMD's Opening
 Markman Brief at 11 (citing Ex. 10 ("Neikirk Deposition")) at 114).

26 ³ Oki's expert describes interleaving with a useful analogy. One might imagine a two
 27 lane road on which cars travel side by side. If the cars each represents a unit of data, this two-
 28 lane road would allow parallel transmission. However, if the two-lane road merges into a single
 lane, the cars will have to enter the single lane "in an alternating manner, one at a time, to avoid
 collision." This merger is analogous to interleaving. Oki's Response to AMD's Opening
 Markman Brief, Ex. 16 ("Oklobdzija Decl.") at ¶ 5.

Opening Markman Brief at 24. Thus, the Court must determine whether multiplexing as used in the Johnson patent requires interleaving. It does.

1. The Claims of the Johnson Patent

Claim 55 describes a method for transferring data back and forth between a computer's CPU and peripheral devices such as printers. "[H]igh performance devices including at least one" CPU are connected to a "first bus." '672 Patent col.49 ls.43-45. "[L]ower performance devices" are connected to a "second bus." Id. at ls.46-47. A "direct memory access means" transfers data between the two buses. Id. at ls.49-50. The "direct memory access ["DMA"] means" includes "at least one direct memory access channel means." Id. at ls.50-52. When the DMA means transfers data between the two buses, the "direct memory access channel means" isolates the CPU (and other high performance devices) from the lower performing devices. Id. at ls.53-57. A second "means," an "input/output ["I/O"] controller means," also transfers data between the two buses. Id. at ls.58-59. The I/O controller means includes "at least one address mapped input/output port means." Id. at ls.59-61. When the input/output controller means transfers data between the two buses, the address mapped input/output port means isolates the CPU (and other high performance devices) from the lower performing devices. Id. at ls.62-66. As the DMA means and the I/O controller means transfer address signals and data signals to the second bus, Claim 55 requires "multiplexing [of the] address signals . . . together with [the] data signals." Id. at col.49 ls.66-67; col.50 ls.1-2.

The claims standing alone are not conclusive on the meaning of multiplexing. However, the claims provide two hints whose implications become fully clear when the claims are read in light of the specification. First, whatever multiplexing is, Claim 55 only requires it as data travels in one direction. Claim 55 refers to data that travels in two directions: from the high performance devices on the first bus to the low performance devices on the second bus, and vice versa. Id. at col.49 l.43. However, Claim 55 only requires multiplexing as data is being transferred to the second bus. Id. at col.49 ls.66-67; col.50 ls.1-2. The second hint is the plain language of the claims themselves. The claims do

not require multiplexing address signals and data signals. The claims require “multiplexing address signals . . . together with data signals.” Id. at col.49 ls.66-67; col.50 ls.1-2. The implications of these hints will become clear as the Court delves into the specification.

2. The Specification of the Johnson Patent

The specification ties together the loose strings left by Claim 55. Two references to multiplexing prove informative. The first occurs in the description of a specific embodiment of the invention. In this embodiment, the bus connected to the high performance devices is actually composed of “two 32 bit wide buses referred to as the ‘Address Bus’ and ‘Data Bus.’” Id. at col.1 ls.35-36. The Johnson patent refers to these two buses collectively as the Local Bus. Id. at 36-38. Address signals travel into a data transfer controller (“DTC”) on the data bus. Id. at fig.3. Data signals travel into the DTC on the data bus. Id. These signals travel either to the input/output ports or the DMA channels. Id. Specifically, the address bus feeds address signals into both the I/O ports and the DMA Channels. Id. Likewise, the data bus feeds data signals into both the I/O ports and the DMA Channels. Id. At this point, then, both the I/O Ports and the DMA Channels are each ready to send a pair of address and data signals traveling in parallel to the remote bus. AMD argues that the multiplexing that Claim 55 refers to is selecting which of the pairs of signals to send to the Remote Bus. AMD’s Opening Markman Brief at 23.

However, that’s not what the specification says. The pairs of signals coming from the local bus to which the high performance devices are connected contain 64 bits of information. Id. at col.1 ls.34-35. However, in the preferred embodiment, the Remote Bus onto which the data must be sent is only 32 bits wide⁴. Id. at col. 8 l.43. Thus, the address signals and the data signals must be interleaved if they are to transfer to the 32 bit Remote Bus. The specification describes this interleaving as the multiplexing: “Fig. 3 goes on to show multiplexing and transceiver circuits . . . to indicate that address signals and data signals are interleaved when output to or received from the Remote Bus.” Id. at col.11 ls.60-

⁴ This is analogous to cars traveling onto a 64 lane highway merging into a 32 lane highway.

64. The specification does not describe multiplexing as choosing between data from the I/O ports and the DMA channels. Thus, the specification indicates that multiplexing, as used in Claim 55, does require interleaving.

Now, the first hint from the claims make sense. Multiplexing only needs to occur when data is transferred in one direction because data only needs to be interleaved as it is transferred from the faster 64 bit bus onto the 32 bit remote bus⁵. This is borne out by the second important reference to multiplexing in the specification: the “Remote Address/Data Bus . . . is a bidirectional, Input/Output; asynchronous/synchronous, three state bus. The signals on this bus are multiplexed address/data signals for Remote Bus 120.” *Id.* at col.8 ls.43-46. The phrase multiplexed address/data signals, like the words together with, invokes the notion that the data have been combined, or interleaved together. However, when describing the data on the Local Bus, the specification does not describe the data as multiplexed. This is so because, as Claim 55 indicates, multiplexing only needs to occur as data is being transferred from the Local Bus to the Remote Bus.

The second hint from Claim 55 also reveals its import when read in light of the specification. The words “together with” suggest that the address signals and data signals are somehow being combined. AMD’s construction of the word multiplexing does not comport with this suggestion. According to AMD, two address-data pairs present themselves to the multiplexer. The multiplexer then chooses which of the two pairs to send on to the Remote Bus. Because each address-data pair arrives in parallel and leaves in parallel, no combination ever occurs. This, however, contradicts the notion that address signals must be multiplexed together with data signals. Interleaving, on the other hand, gives full meaning to the phrase “together with.” According to the correct construction of Claim 55, paired address-data signals present themselves to the multiplexer. The multiplexer then breaks up the data pairs and sends them in time interleaved fashion. This allows address and data signals that arrived on two separate lines to leave the multiplexer on one single line, i.e. the

⁵ Of course, the invention is not limited to a device in which the first and second buses are 64 and 32 bits wide. But the requirement imposed by multiplexing does envision a first bus with a greater data width than the second.

1 remote bus. Construing multiplexing as interleaving gives full meaning to the words of
2 Claim 55.

3 Another part of the specification reveals that the multiplexing as it is used in Claim 55
4 does not refer to selecting whether to send a pairs of signals from the I/O ports or the DMA
5 channels to the Remote Bus. In a section explaining the function of the I/O ports, the
6 specification explicitly refers to process AMD alleges constitutes multiplexing. “If a request
7 from an I/O port for the Remote Bus occurs at the same time as a request from a DMA
8 channel, the I/O has priority.” Id. at col.25 ls.21-23. Unlike interleaving, the specification
9 does not call this process multiplexing. The specification does not state that this activity is
10 conducted by a multiplexer. Thus, while the patentee contemplated that the invention would
11 make this decision between pairs of signals, he did not call it multiplexing.

12 AMD suggests that a reference to multiplexing in the specification’s description of
13 Figure 8 impacts the Court’s construction of multiplexing in Claim 55. AMD’s Opening
14 Markman Brief at 24. The Court disagrees. Figure 8 of the specification depicts a block
15 diagram of a DMA channel described by Claim 14. Compare id. at col.30 ls.11-23 with
16 col.44 ls.49-68. Claim 14 refers to multiplexing that takes place within the DMA channel.
17 Both parties agreed at oral argument that this type of multiplexing does not require
18 interleaving. Instead, this multiplexing does what AMD wishes the multiplexing in Claim 55
19 would do: it selects between two inputs that must be presented one at a time to a single
20 output. Id. at col.44 ls.52-57. While this use of multiplexing does reveal that the patentee
21 knew that the word multiplexing, in the abstract sense, could have many meanings, it does
22 not inform the interpretation of Claim 55. Both the language of Claim 14 and the portion of
23 the specification describing this multiplexing use different terminology than Claim 55.
24 Claim 14 depends from Claim 13, which describes a data transfer controller that has a “queue
25 means for buffering data being sent between the first and second bus.” Id. at ls.45-46. Claim
26 14 then goes on to add the further limitation that the device set forth in Claim 13 have “(a)
27 first multiplexing means for selectively transferring word length data input to [the] access
28 means from [the] first bus and for selectively transferring packed data, input to [the] access

means from said packing and funneling network means, into [the] queue means.” Id. at col.44 ls.52-57. Two important differences between Claim 14 and Claim 55 are apparent. When the patentee uses multiplexing to describe the selection of one of two pieces of data, the claim explicitly describes that choice. Furthermore, Claim 14 does not state that the invention multiplexes “word length data” together with “packed data.” Instead, the Claim uses language that indicates that the device is selectively choosing between them. Thus, the construction of multiplexing in Claim 55 is not altered by the fact that other claims indicate that the invention multiplexes in different ways.

The construction of Claim 55 in the Johnson patent reveals how the world of claim construction has changed since the Federal Circuit issued its landmark decision in Phillips. Prior to that decision, claim construction would begin with the various definitions of multiplexing the parties have offered. Phillips, 413 F.3d at 1319. Then, a court would attempt to look for an explicit indication in the patent that these definitions fell outside its scope. Id. Were the Court to engage in this method of claim construction, it might construe multiplexing to include interleaving and selecting between pairs of data since there is no explicit statement in the Johnson patent that this cannot be so. However, the Federal Circuit has rejected this method of claim construction. Id. at 1320. Instead of beginning with broad dictionary definitions, the Court begins with the language of the Johnson patent itself, allowing the claims and the specification to define the scope of the term multiplexing. See id. This method ensures that the Court does not construe multiplexing in an overly expansive way. See id.

3. Construction of Disputed Terms in the Johnson Patent

Based upon the foregoing considerations, the Court construes the phrase “multiplexing address signals being transferred to said second bus by said access means and said controller means, together with data signals being transferred to said second bus” in Claim 55 of the Johnson patent as follows: Address and data signals are being transferred to the second bus by the access and controller means. In this step, those address and data signals are combined for transmission over the second bus.

IT IS SO ORDERED.

Dated: February 14, 2006



CHARLES R. BREYER
UNITED STATES DISTRICT JUDGE

United States District Court

For the Northern District of California